REMARKS

This Amendment, submitted for filing with an RCE being filed concurrently herewith, is responsive to the Final Office Action mailed February 13, 2008.

In accordance with the foregoing, claims 1, 5, 9, 11, 13, and 14 are amended and new claim 16 is presented. No new matter is presented in any of the foregoing and, accordingly, approval and entry are respectfully requested.

Claim Amendments

Claim 1 is amended herein to recite a semiconductor device substrate comprised of a core substrate having, "the core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, . . .and an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer." Claims 5, 9, 11, 13, and 14 are similarly amended.

Support for the amendments is found for example in paragraphs [0020] -[0023] of the specification. No new matter is presented in any of the foregoing and, accordingly, approval and entry are respectfully requested.

Final First Office Action Would Not Be Proper

On April 22, 2008, Applicants filed a Letter To the Examiner and Request For Withdrawal of Final Status as Premature ("Letter to the Examiner") in which Applicants submitted that the finality of the current Office Action mailed February 13, 2008 ("current Office Action") is premature since the Examiner's response is incomplete in having not addressed all of the Applicants' arguments in the previous Amendment filed November 9, 2007 ("previous Amendment") traversing the rejections in the previous Office Action mailed August 9, 2007 ("previous Office Action").

As of June 13, 2008, a response to the Letter to the Examiner has not been received by the Applicants.

In view of the arguments presented in the Letter To the Examiner and herein, Applicants respectfully submit that if the case is not found in condition for allowance, a first Office Action that is a final first Office Action would not be proper.

Item 4: Rejection Of Claims 1-10 under 35 U.S.C. §103(a) as being unpatentable over Abe (Pub. No. US 2003/0136677)

In Item 4 of the Office Action, the Examiner rejects claims 1-10 under 35 U.S.C. §103(a) as being unpatentable over Abe. (Action at pages 3-5). The rejection is traversed.

Independent claim 1 recites a semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein: "the core substrate being of a material having a heat expansion coefficient of 4.0 to 10.6 ppm/^{0}C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, and a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate, an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer." Independent claims 5 and 9 have similar recitations.

That is, according to an embodiment of the present invention, the core substrate has on both sides --outermost layers formed of a resin layer and having a higher strength and a higher elongation than a resin material of inner resin layers of the core substrate.

Thus, according to an embodiment of the present invention, outermost layers of the resin layer can suppress (from both sides of the semiconductor device substrate) a thermal stress generated between the core substrate and the inner resin layers.

Thus, for example, occurrence of cracking of the inner resin layers and the interconnect patterns can be reduced.

Further, according to an embodiment of the present invention, the heat expansion coefficient can be suppressed over the semiconductor device substrate.

Further, according to an embodiment of the present invention an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate.

Thus, cracking can be reduced from occurring in interconnect patterns - -as being protected by the outermost layer formed of the resin layer, even in the outermost interconnect patterns that can be subjected to a high stress due to, for example, a connection to a semiconductor chip or to a mother board.

By contrast, Abe merely teaches various materials of a circuit board and does not teach nor suggest a use of a material having a specific property at a specific site of the circuit board.

That is, Abe does not teach nor suggest a resin having a high strength and elongation used as a outermost resin layer.

Further, Abe does not teach that the specific characteristics of strength and/or elongation are different respectively for an outermost resin layer and inner resin layer.

The Examiner asserts:

> it is prima facie obvious to an artisan for optimization and experimentation to select the available materials.

(Office Action, page 3).

But, Applicants submit that the Examiner's assertion must be viewed in context of Abe's teaching, for example, that:

> [C]arbon fibers arranged in the core layer include a first and a second carbon fiber groups which are arranged in different direction to intersect each other, whereby a thermal expansion coefficient and strength of the core layer can be adjusted for arrangement directions of the first and the second carbon fiber groups by arranged amounts and cross angles of the first and the second carbon fiber groups. The thermal expansion coefficient and strength of the circuit board can be adjusted corresponding to electronic parts to be mounted.

(See, for example, paragraph [0019]).

That is, Abe teaches an adjustment of properties of a core layer by using different arrangements of carbon fibers, and not by using an adjustment of resins.

Applicants submit that that a person of ordinary skill in the art would not have modified Abe as the Examiner asserts. In particular, Abe teaches:

> [T]he thermal expansion coefficients of invar, covar, alloys, such as silicon steel, and a clad material, such as CIC, are substantially the same as the thermal expansion coefficient of silicon. However, they have large specific gravities and add weights unsuitably to be used in the circuit boards, which are processed with the large-sized cores included. Their Young's moduli of elasticity are not high, and large core substrate(s) undesirably have bowing and waves, which causes troubles in the build-up process and in mounting

semiconductor elements.

(Emphasis added, see, for example, paragraph [0010]).

That is, Abe teaches that a core, as recited by claim 1, for example, including a "substrate being of a material having a heat expansion coefficient closer to that of a semiconductor chip" is unsuitable. Abe teaches, instead, a core substrate that is a fiber reinforced metal, and different compositions and rearrangements of a core by rearranging carbon fibers, for example.

Applicants submit that one of ordinary skill in the art would not modify Abe, which teaches adjusting thermal coefficients and strengths of a core layer by rearranging carbon fibers, to substitute a core that Abe teaches is undesirable and unsuitable and select relative resin compositions and respective orientations as recited by claim 1, for example.

Applicants submit this traversal meets the Consideration of Applicant's Rebuttal Evidence Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in *KSR* International Co. v. Teleflex Inc. of October 3, 2007 and the elements in combination do not merely perform the function that each element performs separately, and the results of the claimed combination were unexpected.

Summary

Since features recited by independent claims 1, 5, and 9 (and respective dependent claims) are not taught by even a combination of the art relied on by the Examiner, the rejection should be withdrawn and claims 1-10 allowed.

Item 5: Rejection of claims 11-15 under 35 U.S.C. §103(a)

In item 5 at pages 5-6 of the current Office Action, the Examiner rejects claims 11-15 as being unpatentable over Abe in view of art Nair (U.S. Pub. 2004/0095734). The rejection is traversed.

Independent claim 11 recites a semiconductor device substrate comprised of a core substrate having, on both main surfaces of which, respective interconnect patterns extending through resin layers, wherein: "a core substrate being of a metal alloy having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, the heat expansion coefficient closer to that of a semiconductor chip than the respective heat expansion coefficients of the resin layers and the interconnect patterns, and a resin layer, forming an outermost layer of the semiconductor device substrate on each of the main surfaces thereof, of a material having at least one of a higher strength and a higher elongation than a resin material used for inner resin layers of the

semiconductor device substrate and preventing cracking and deformation, of the semiconductor device substrate due to thermal stress occurring between two or more of the core substrate, the inner resin layers, and the interconnect patterns in the semiconductor device substrate, an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern has a land exposed through the outermost layer formed of the resin layer." Independent claims 13 and 14 have similar recitations.

As discussed in traversing the rejection of claims 1-10 above, Applicants submit that:

- Abe does not teach nor suggest a core substrate being of a metal alloy having a heat expansion coefficient of 4.0 to 10.6 ppm/^{0}C, and

- Abe does not teach nor suggest an outermost interconnect pattern of the semiconductor device substrate is coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern has a land exposed through the outermost layer formed of the resin layer.

Applicants submit that Nair, relied on by the Examiner as teaching a core substrate made of an iron nickel alloy, does not overcome the deficiencies in the teachings of Abe discussed above.

In addition, the Examiner asserts that Nair teaches:

> an analogous device having a core substrate . . . made of an iron-nickel alloy . . . for providing a high capacitance substrate. . . obvious . . . to [sic- modify] material of the core substrate of Abe with the iron nickel alloy material, as taught by Nair, for providing the advantage.

(Action at page 5).

But, Applicants further submit the Examiner's assertions regarding Nair must be viewed in context of Abe that specifically discloses:

> As shown in Table 1, the thermal expansion coefficients of the metal materials are larger than the thermal expansion coefficient 3.5 ppm/.degree. C. of silicon, but the thermal expansion coefficient of carbon is 0 2 ppm/.degree. C., which is smaller than that of silicon. The thermal expansion coefficient of SiC is substantially equal to that of silicon. . . . found that a composite material of the metal material and the fiber material is formed to thereby form the core substrate of a thermal expansion coefficient which is approximate to that of silicon.

(Emphasis added, See, paragraph (0053)).

That is, Abe teaches that a metal alloy has a thermal coefficient expansion that is larger than the thermal expansion coefficient of silicon and, for a core substrate to have a thermal

expansion coefficient substantially equal to that of silicon, the core substrate needs to be a composite material.

Thus, Applicants submit that one of ordinary skill in the art would not have combined Abe and Nair, in a manner as the Examiner suggests.

Applicants submit the recited elements in combination do not merely perform the function that each element performs separately, and the results of the claimed combination were unexpected.

Summary

Since features recited by independent claims 11, 13, and 14 (and dependent claims 12 and 15) are not taught by even an *arguendo* combination of the art relied on by the Examiner, the rejection should be withdrawn and claims 11-15 allowed.

Examiner's Assertions Not Properly Supported

In the previous Amendment, Applicants argued there is no "rational underpinning" to support the modification of Abe as the Examiner asserts, and the Examiner's assertions that "resin layers . . . may be selected among the disclosed group of materials . . . so as to provide the outermost layer with the higher strength and elongation than the inner layer because the results are (merely) predictable" are merely conclusory and without articulated reasoning.

In addition, Applicants argued by contrast, Abe's teachings are directed to a core substrate "formed of a fiber reinforced metal," and advantages over the prior art are directed to Abe's teaching of a use of fibers. Applicants further argued that while the Examiner asserted that it would have been obvious to modify Abe for "preventing cracking" Abe does not address cracking, at all.

But, in the current Office Action, the Examiner does not address these arguments, but merely asserts:

> A semiconductor substrate may be made of a silicon substrate, thereby making the core layer suitable for the claimed limitation. . . .the selection of material for the insulating layer is obvious because the result is predictable.

(Emphasis added, Current Office Action at page 6, lines 14-17).

Applicants submit that the Examiner's statement "the result is predictable" is not supported.

As set forth, for example, in MPEP § 2144.03(a) :"the notice of facts beyond the record which may be taken by the Examiner must be "capable of such instant and unquestionable

demonstration as to defy dispute."

Thus, Applicants respectfully submit that if the case is not found in condition for allowance that in view of the above, a first Office Action that is a final first Office Action would not be proper and complete arguments include required support for such a statement, or if the statement is based on the Examiner's personal views, the Examiner provide an affidavit as required under 37 C.F.R. §1.104(d)(2).

Current Action is Incomplete

In traversing the rejection of claims 11-15 in the previous Amendment, Applicants argued the Examiner's assertions regarding a reasonable chance of success to combine the art are in error since Abe specifically teaches a metal alloy has a thermal coefficient expansion that is larger than a thermal expansion coefficient of silicon and for a core substrate to have a thermal expansion coefficient substantially equal to that of silicon, the core substrate needs to be a composite material.

However, in the current Office Action, the Examiner does not address these arguments. Thus, Applicants respectfully submit that if the case is not found in condition for allowance that in view of the above, a first Office Action that is a final first Office Action would not be proper.

New Claim

New claim 16 is presented to recite features of the invention in a different fashion.

New claim 16 recites a semiconductor device substrate including "a core substrate having a heat expansion coefficient of 4.0 to 10.6 ppm/°C, and an outermost interconnect pattern of the semiconductor device substrate coated by a resin layer forming an outermost layer of the semiconductor device substrate, and the outermost interconnect pattern having a land exposed through the outermost layer formed of the resin layer."

Support for these features are found, for example, in paragraphs [0021 and Figure 4 of the specification.

Claim 16 is submitted to distinguish patentably over the art currently relied on by the Examiner, and to be allowable for the recitations therein.

Conclusion

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Serial No. 10/827,318

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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